FIG.1

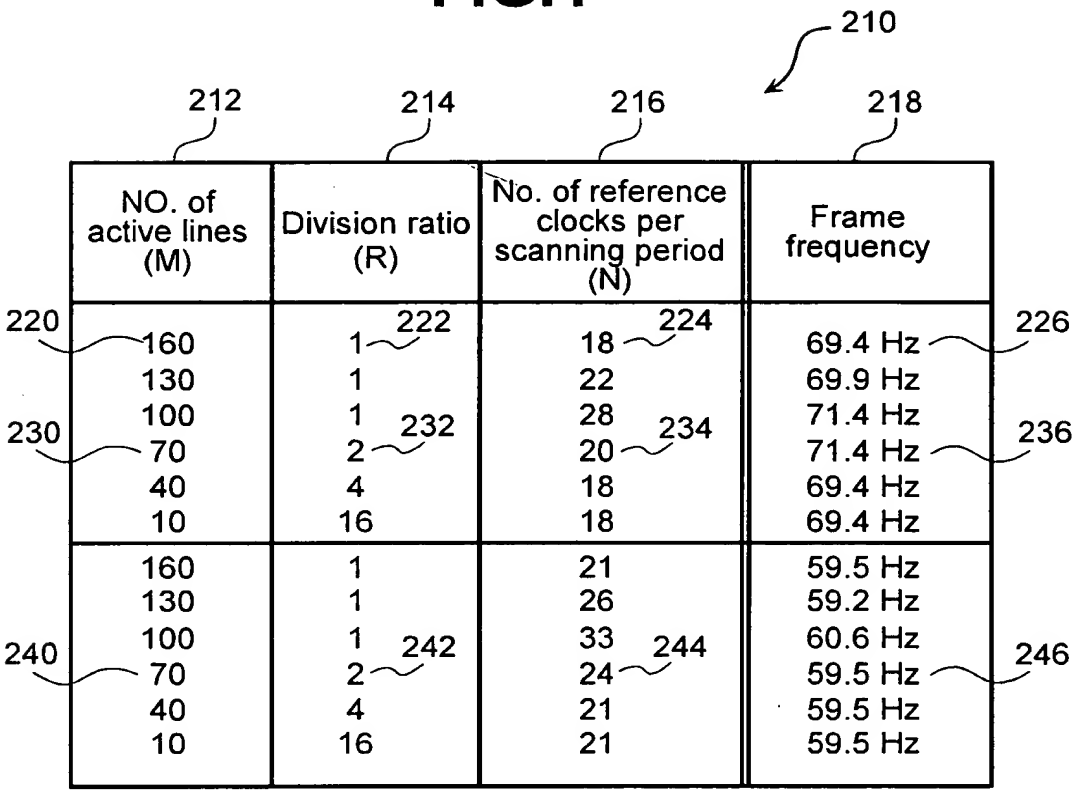


FIG.3

Signal name	Meaning	"Low"	"High"
CS	chip select	accessible	inaccessible
RS	register address/data selection	address	data
E	data write/read activation	active	inactive
RW	data write/read selection	write	read
D	interactive data	—	—

FIG.2

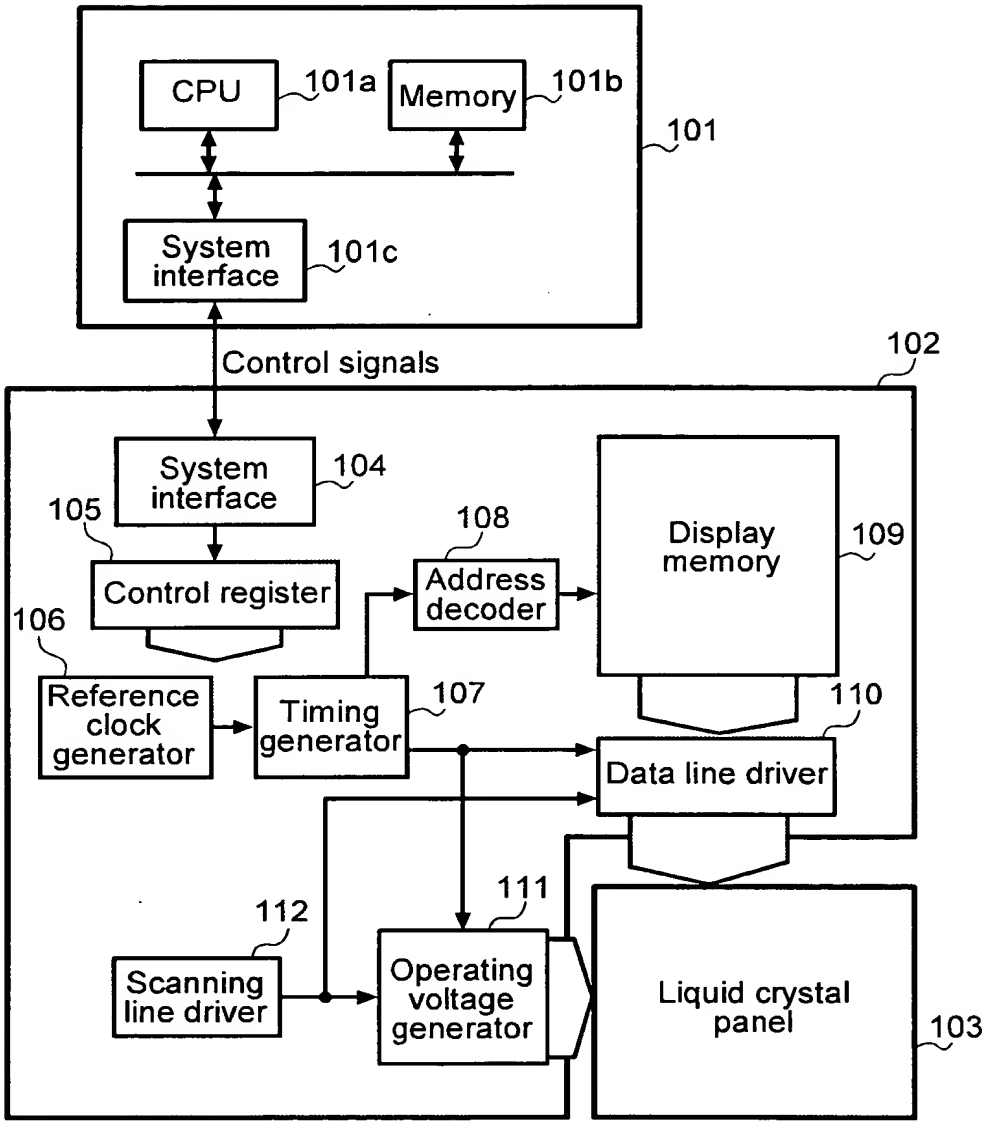

CPU
101a
Memory
101b
101
System interface
101c
Control signals
102
System interface
104
105
Control register
108
Address decoder
Display memory
109
106
Reference clock generator
Timing generator
107
110
Data line driver
111
112
Scanning line driver
Operating voltage generator
Liquid crystal panel
103

FIG.4

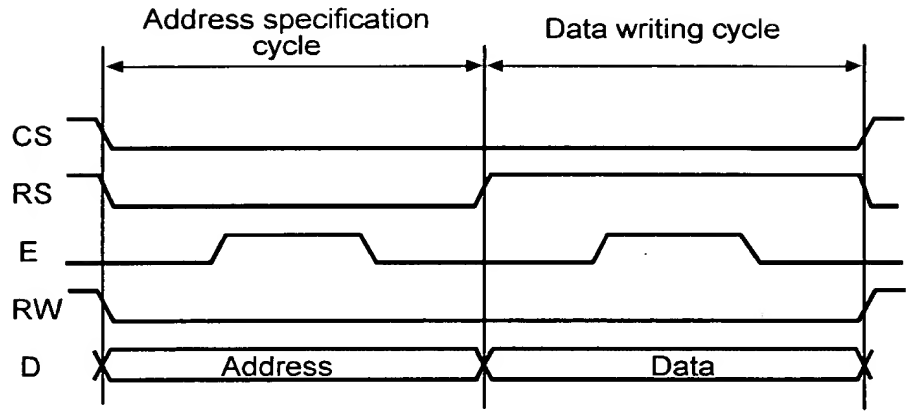

Address specification cycle
Data writing cycle
CS
RS
E
RW
D
Address
Data

FIG.5

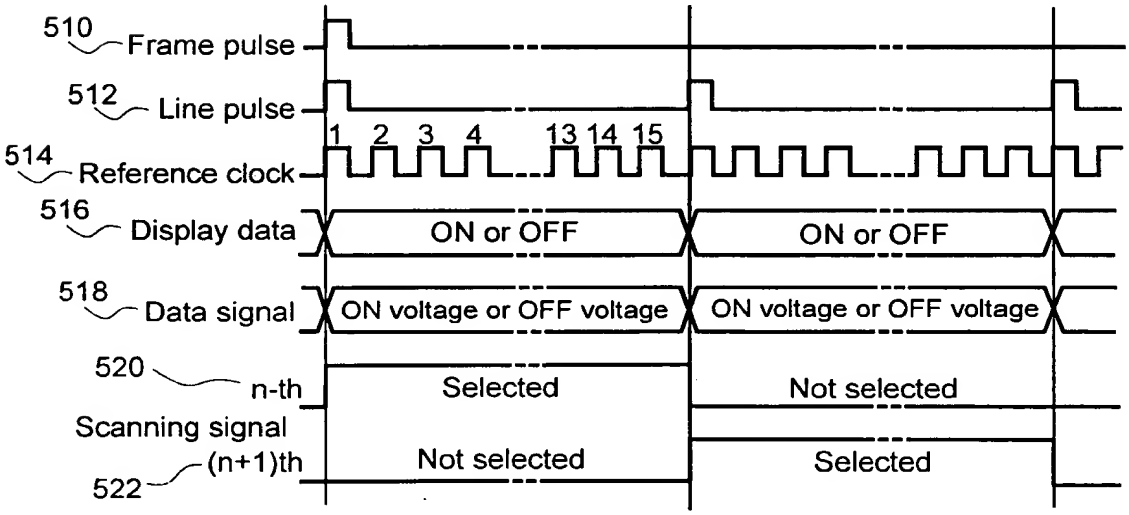

510 Frame pulse
512 Line pulse
514 Reference clock
1 2 3 4 13 14 15
516 Display data
ON or OFF
ON or OFF
518 Data signal
ON voltage or OFF voltage
ON voltage or OFF voltage
520 n-th Scanning signal
Selected
Not selected
522 (n+1)th
Not selected
Selected

FIG.6

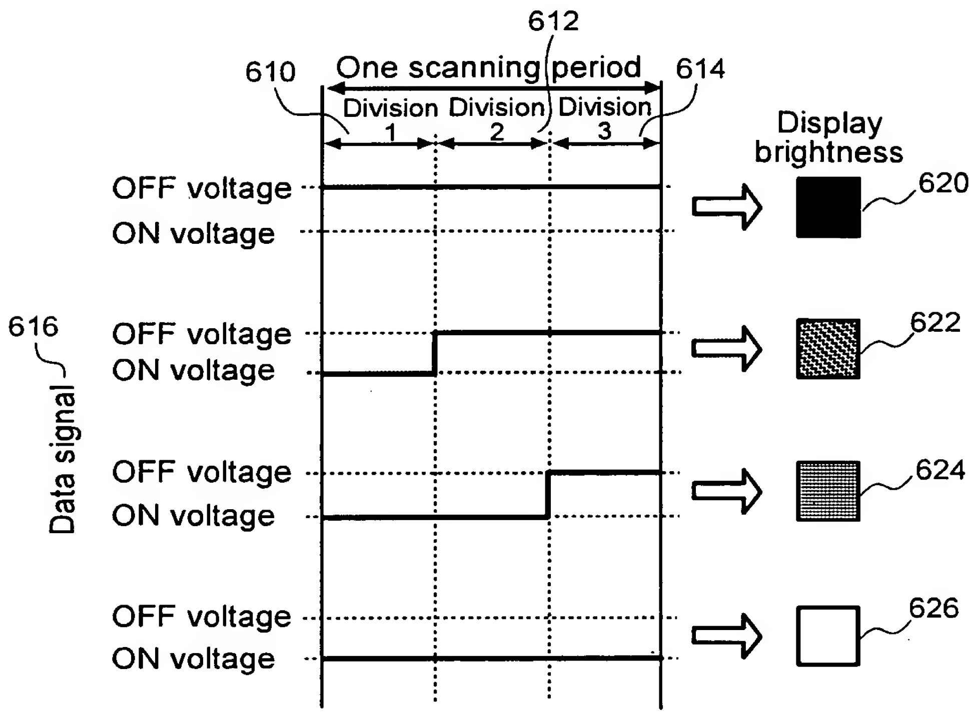

612
610
One scanning period
614
Division 1
Division 2
Division 3
Display brightness
OFF voltage
ON voltage
620
616
Data signal
OFF voltage
ON voltage
622
OFF voltage
ON voltage
624
OFF voltage
ON voltage
626

FIG.7

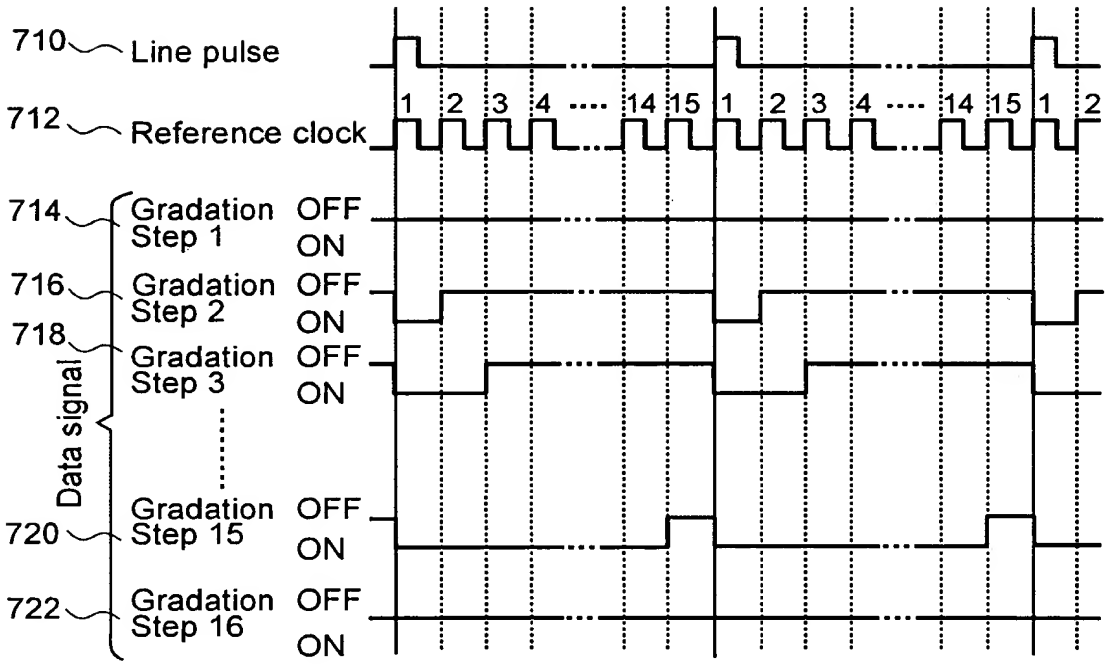

710
Line pulse
712
Reference clock
1 2 3 4 .... 14 15 1 2 3 4 .... 14 15 1 2
714
Gradation Step 1
OFF
ON
716
Gradation Step 2
OFF
ON
718
Gradation Step 3
OFF
ON
Data signal
720
Gradation Step 15
OFF
ON
722
Gradation Step 16
OFF
ON

FIG.8

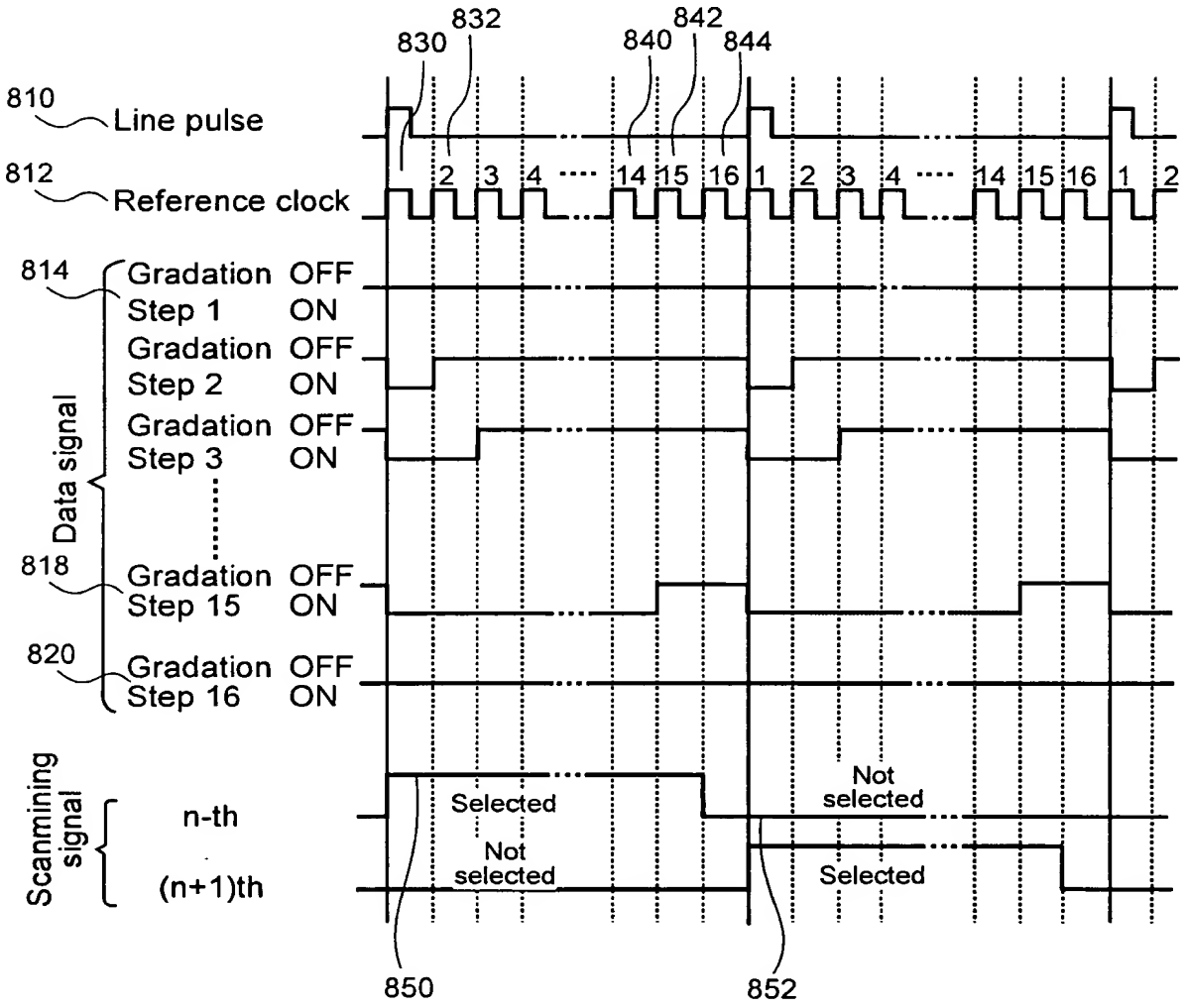

830
832
840
842
844
810
Line pulse
812
Reference clock
2 3 4 .... 14 15 16 1 2 3 4 .... 14 15 16 1 2
814
Gradation OFF
Step 1 ON
Gradation OFF
Step 2 ON
Gradation OFF
Step 3 ON
Data signal
818
Gradation OFF
Step 15 ON
820
Gradation OFF
Step 16 ON
Scanmining signal
n-th
(n+1)th
Selected
Not selected
Not selected
Selected
850
852

FIG.9

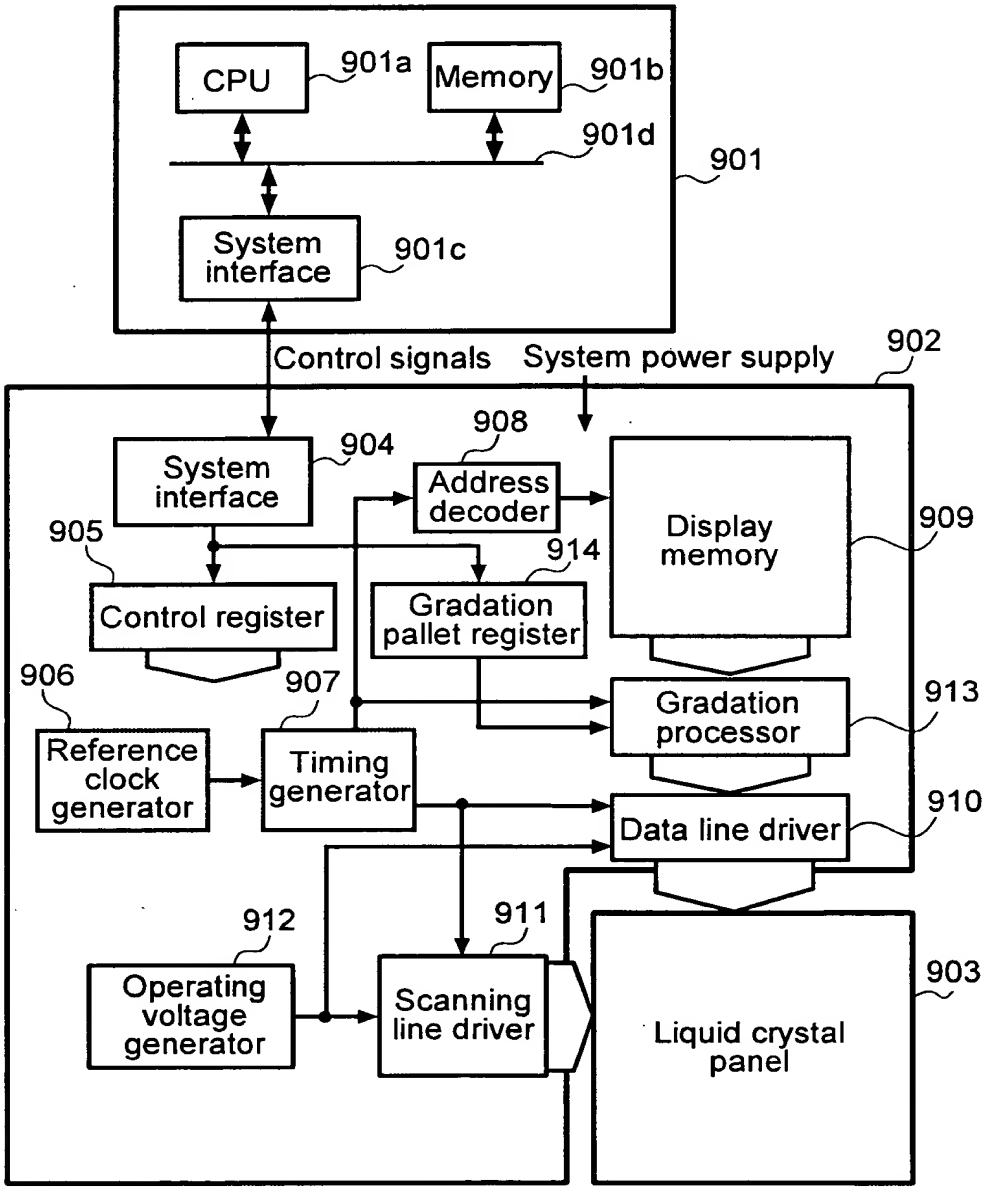

CPU
901a
Memory
901b
901d
901
System interface
901c
Control signals
System power supply
902
System interface
904
908
Address decoder
905
914
Display memory
909
Control register
Gradation pallet register
906
907
Gradation processor
913
Reference clock generator
Timing generator
Data line driver
910
912
911
Operating voltage generator
Scanning line driver
903
Liquid crystal panel

FIG.10

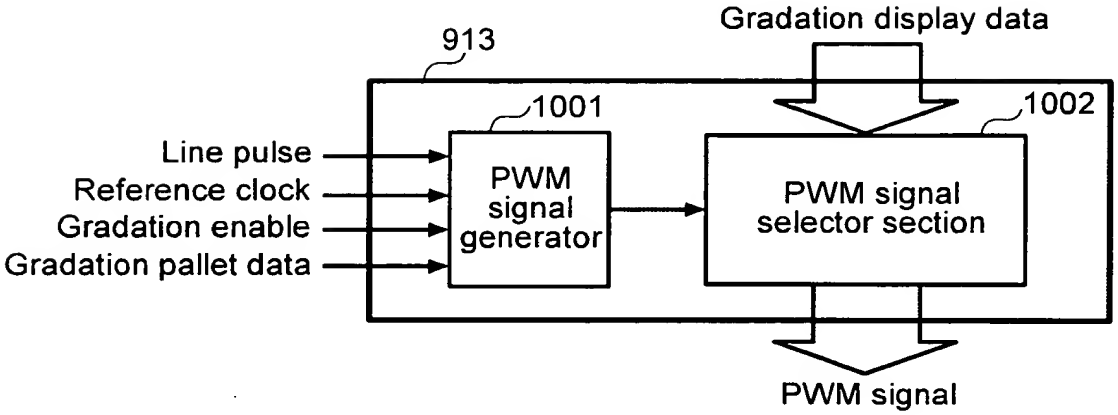

Gradation display data
913
1001
1002
Line pulse
Reference clock
Gradation enable
Gradation pallet data
PWM signal generator
PWM signal selector section
PWM signal

FIG.11

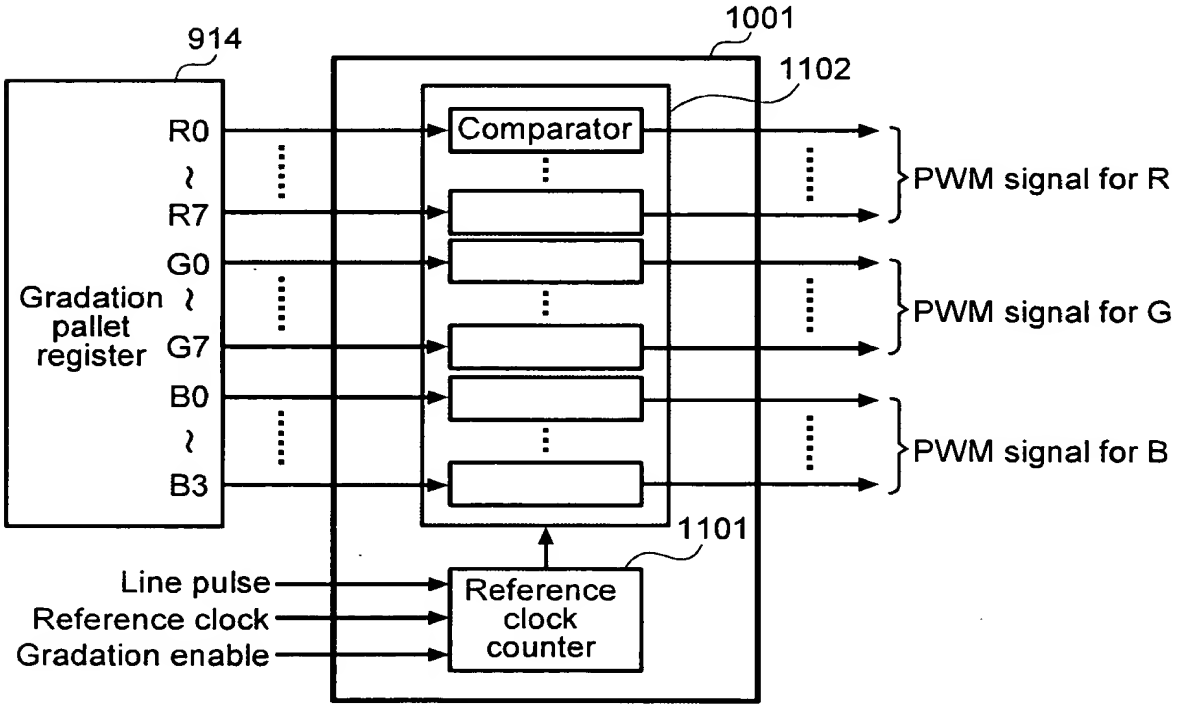

914
1001
1102
R0
R7
G0
G7
B0
B3
Gradation pallet register
Comparator
PWM signal for R
PWM signal for G
PWM signal for B
1101
Line pulse
Reference clock
Gradation enable
Reference clock counter

FIG.12

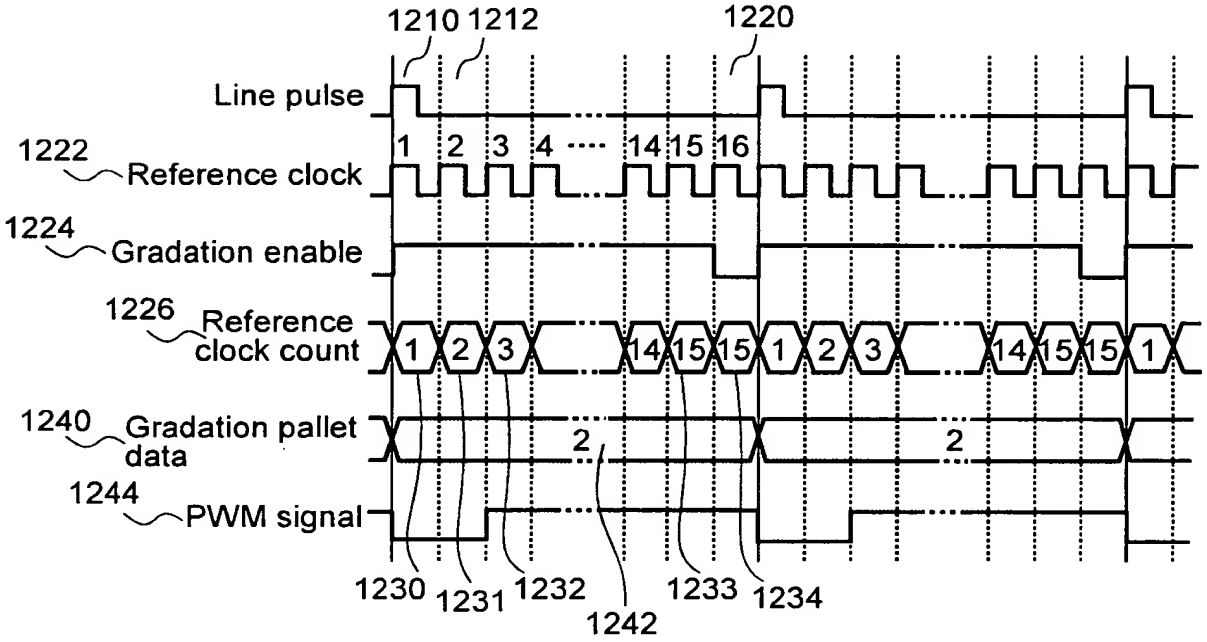


FIG.13

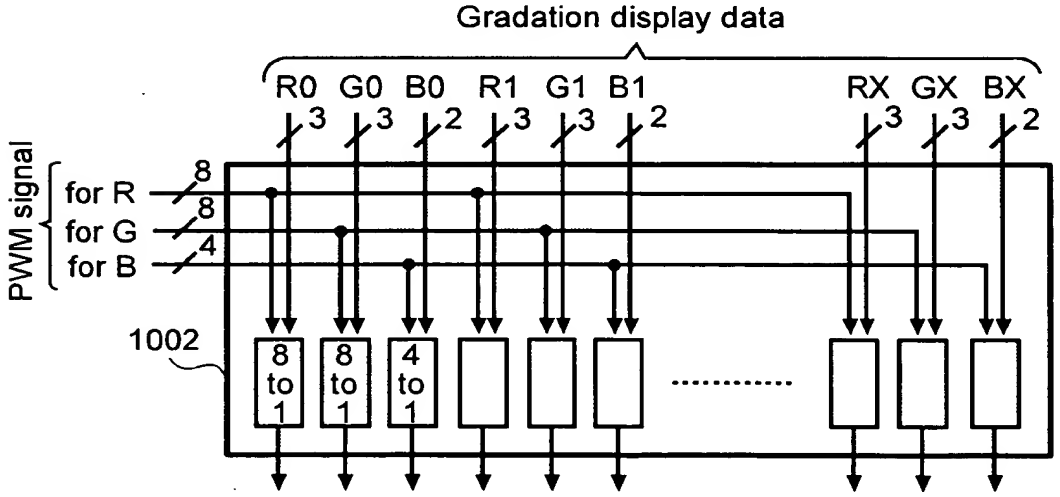


FIG.14

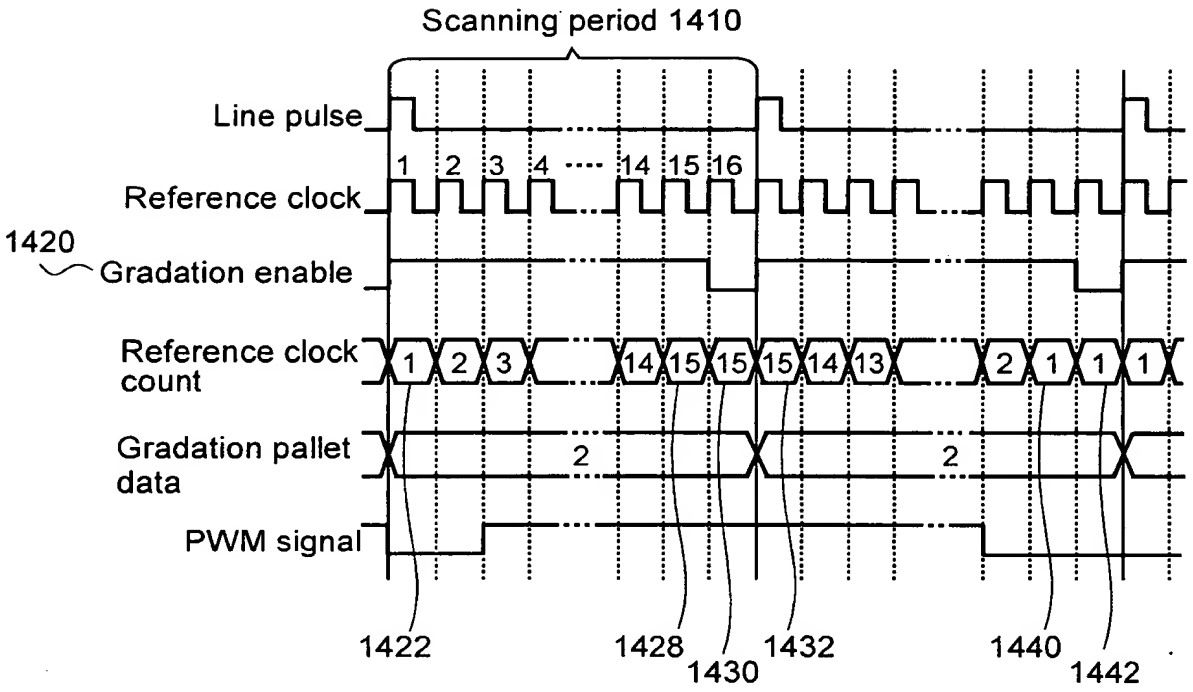
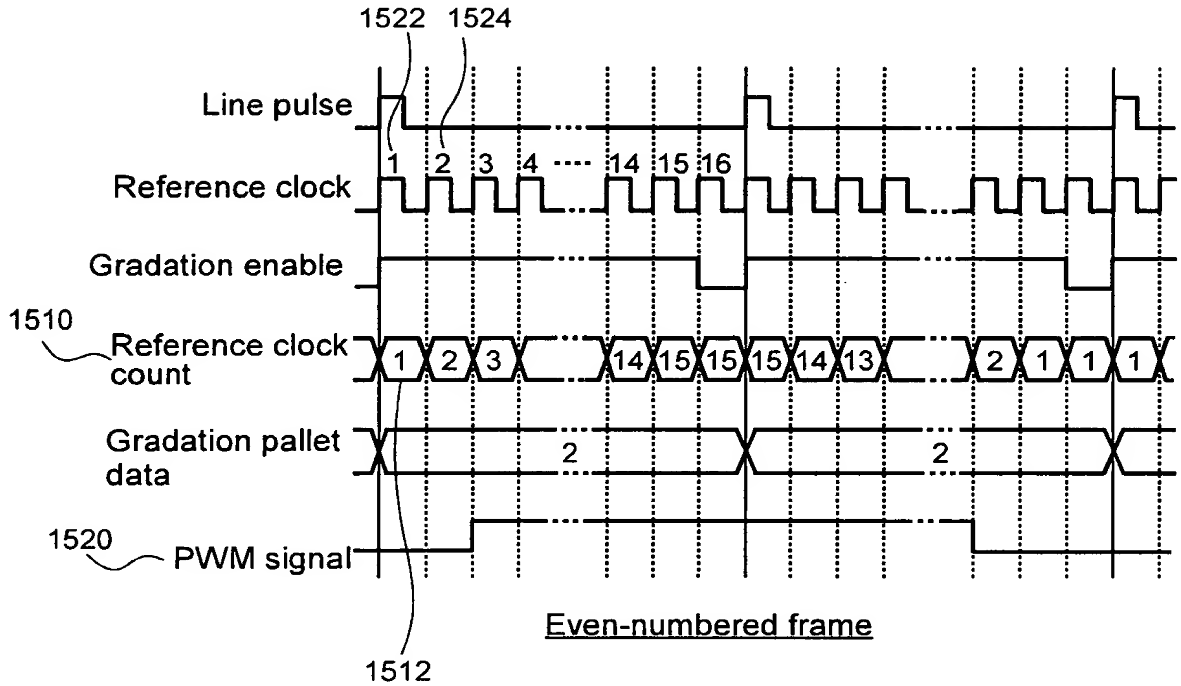


FIG.15a



Even-numbered frame

FIG.15b

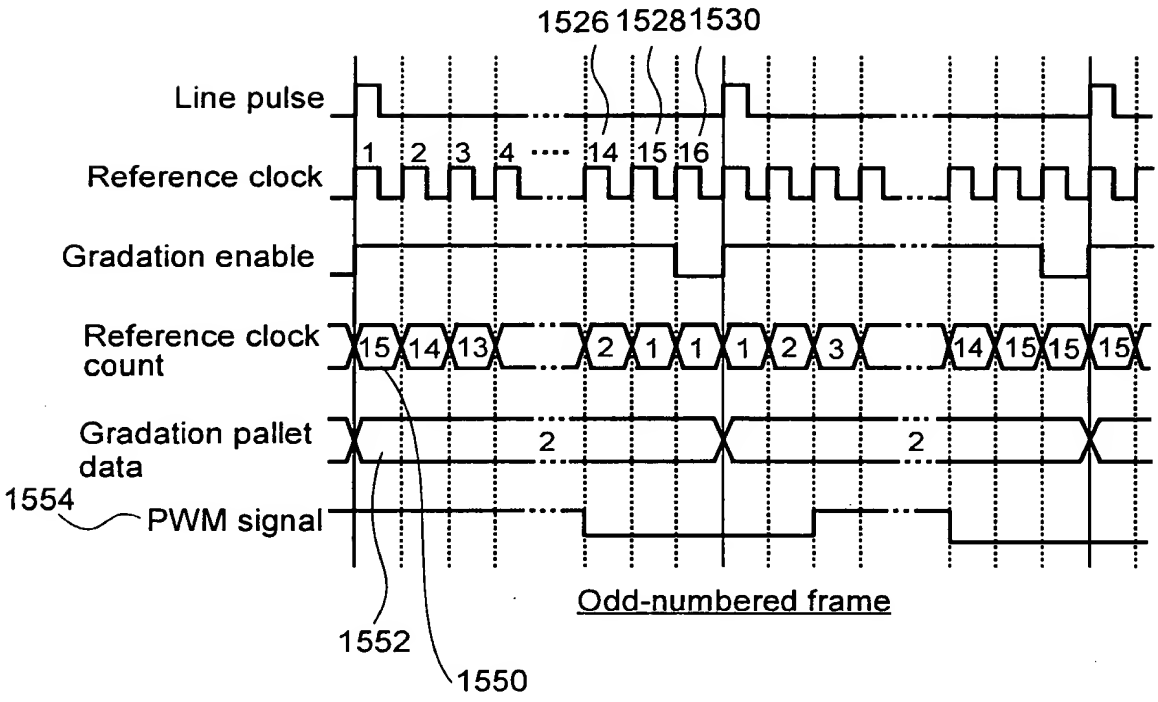


FIG.16

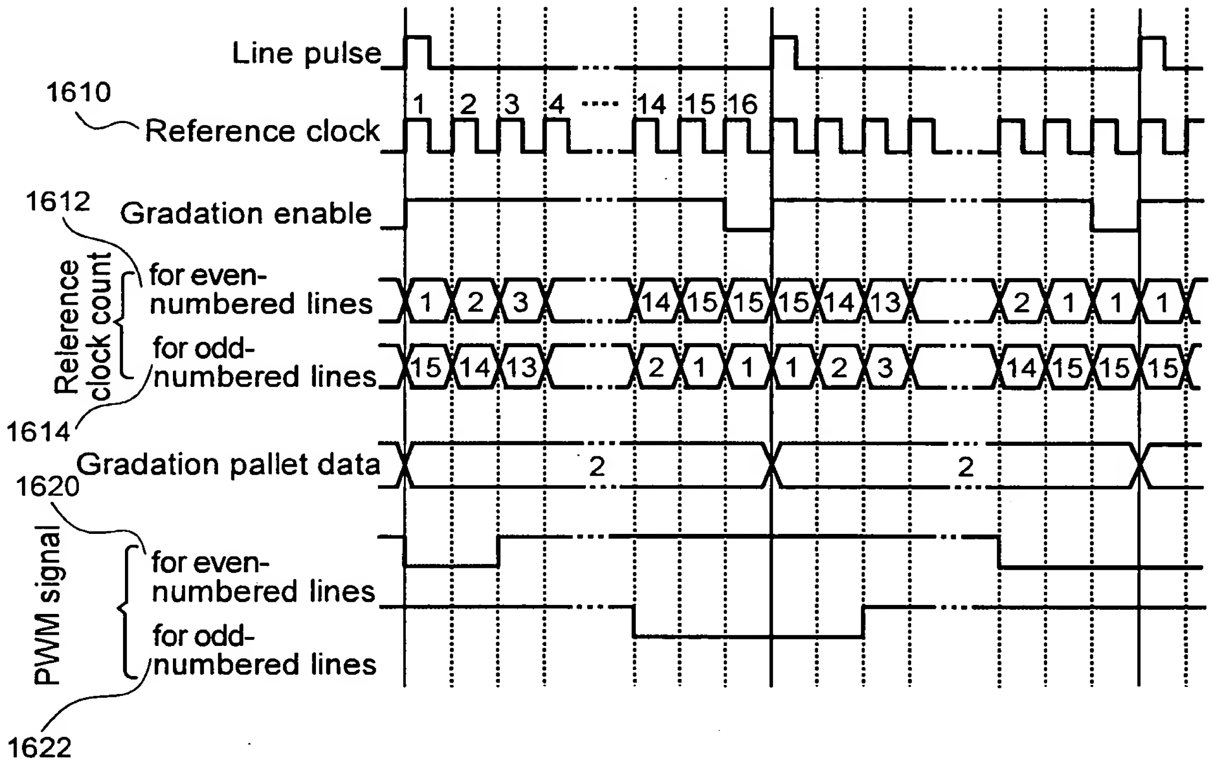


FIG.17

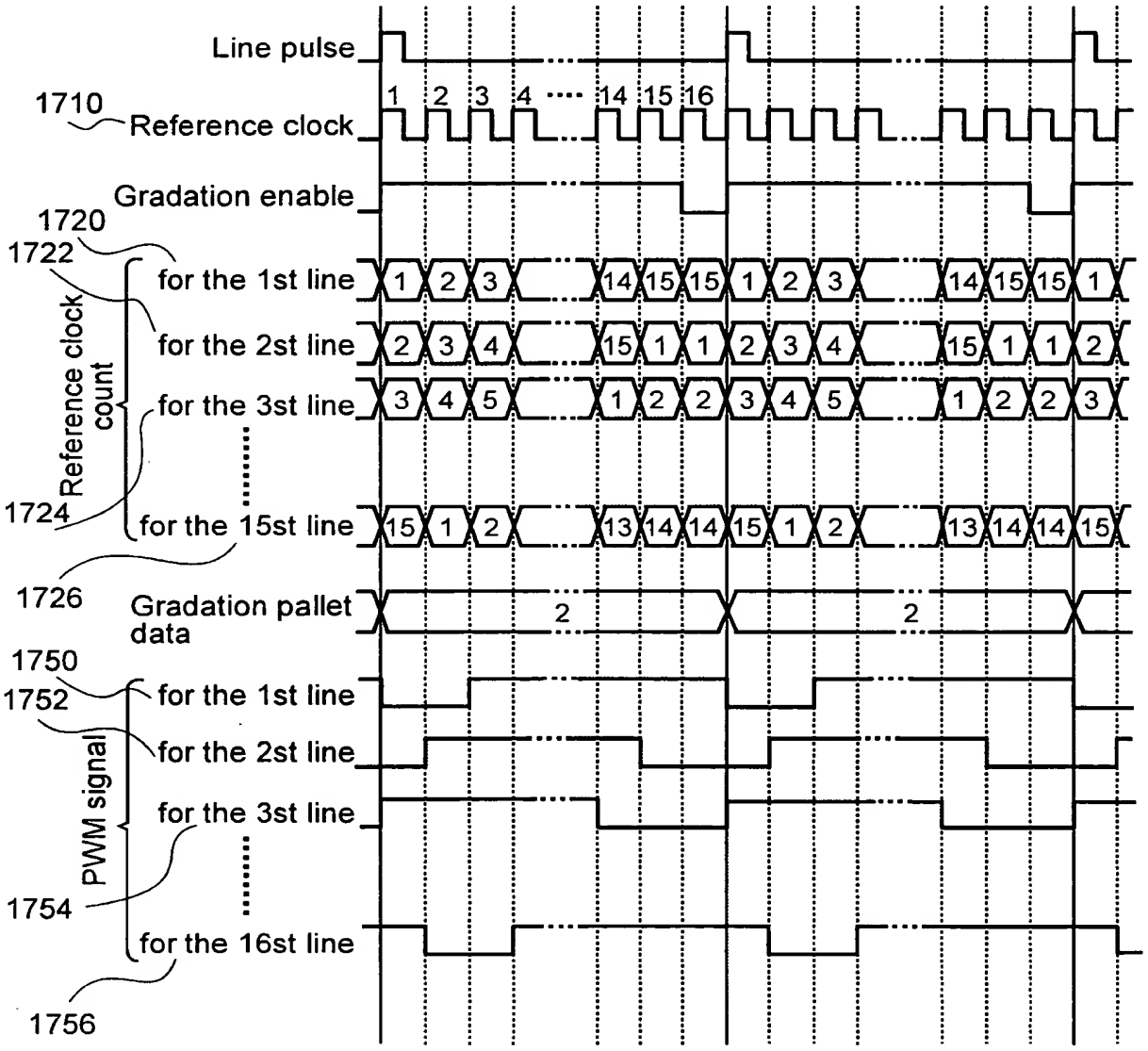

Line pulse
1710
Reference clock
1 2 3 4 ···· 14 15 16
Gradation enable
1720
1722
for the 1st line
for the 2st line
for the 3st line
for the 15st line
Reference clock count
1724
1726
Gradation pallet data
1750
1752
for the 1st line
for the 2st line
for the 3st line
for the 16st line
PWM signal
1754
1756

FIG.18a

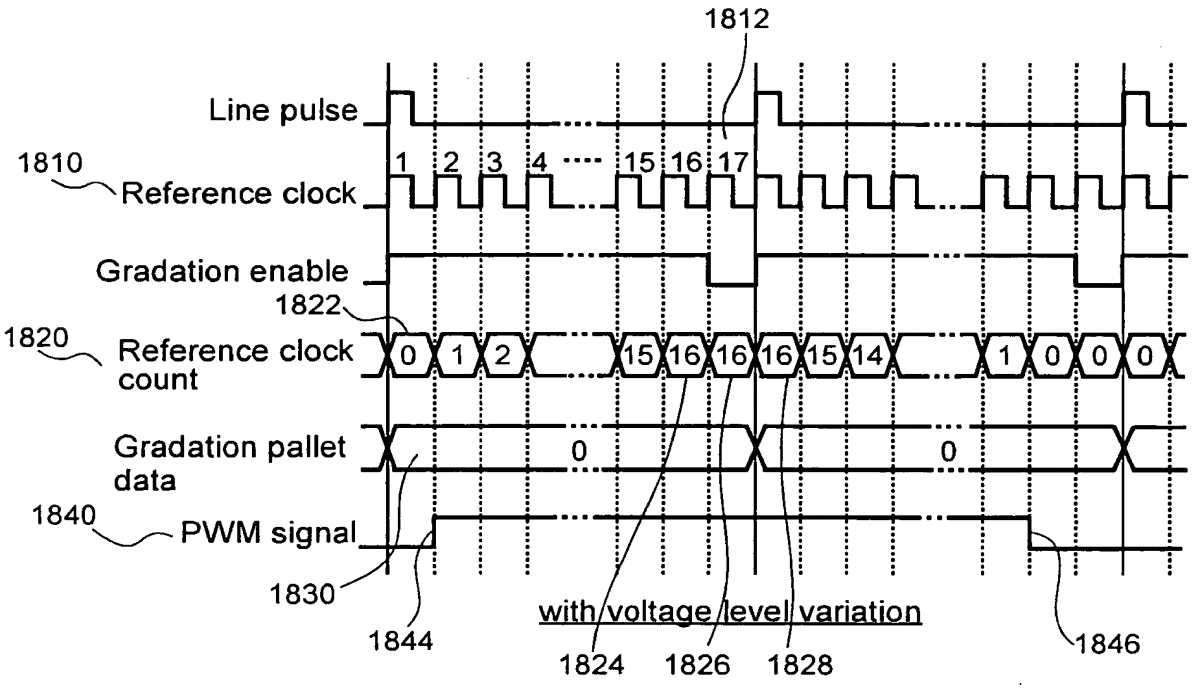


FIG.18b

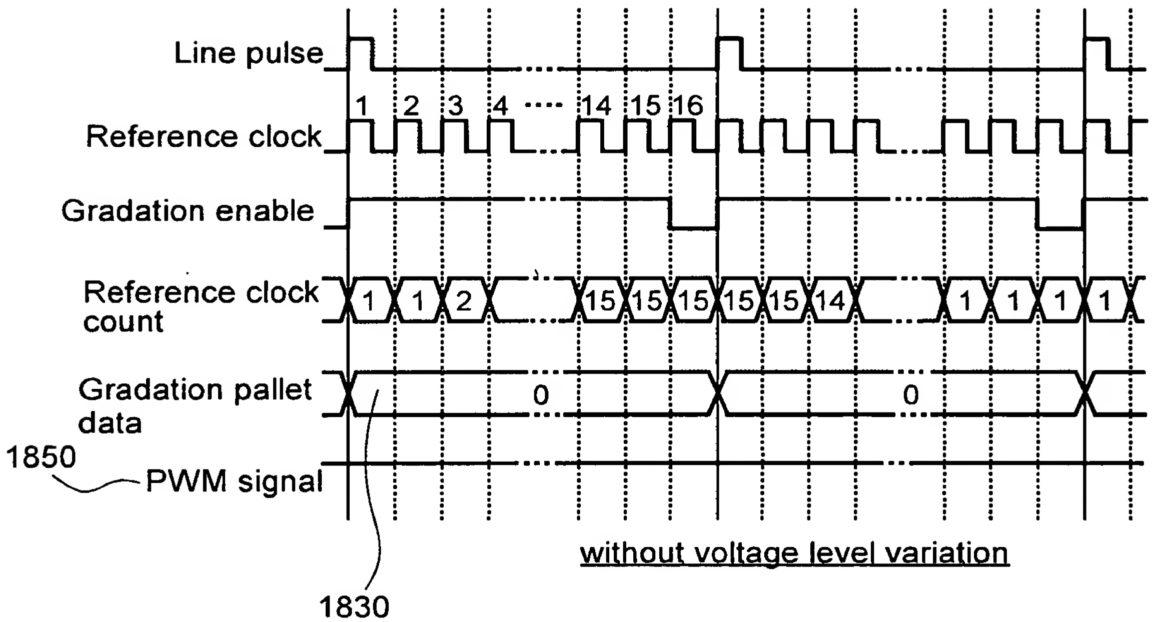
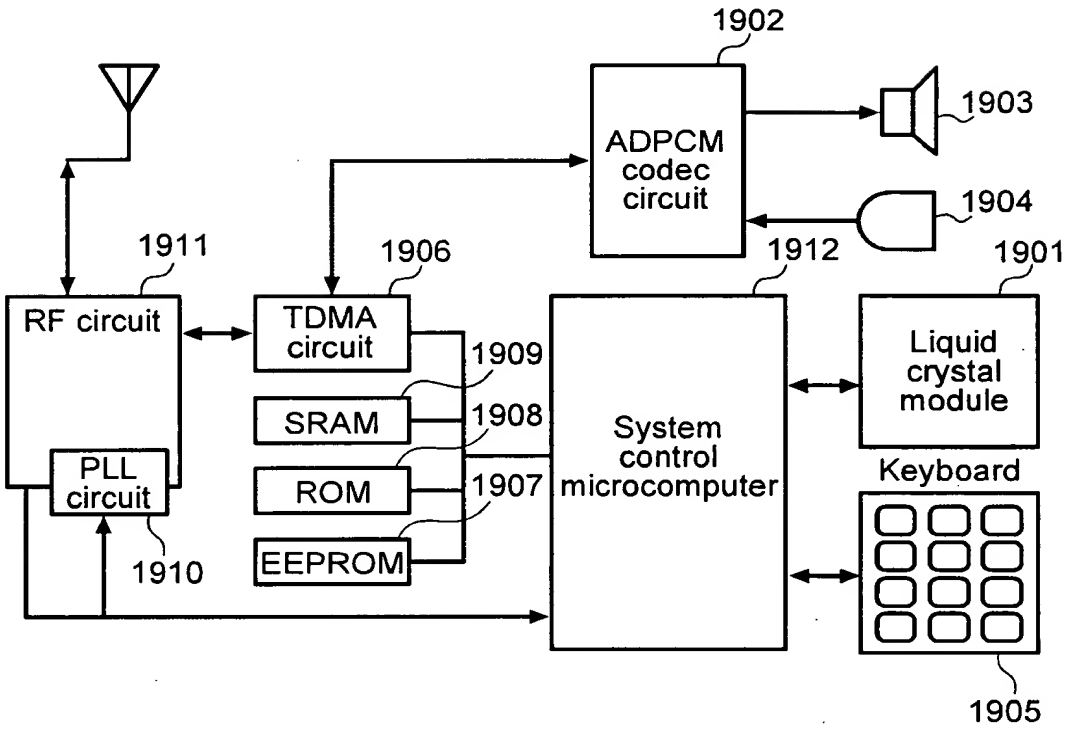


FIG.19


1902
ADPCM codec circuit
1903
1904
1911
1906
1912
1901
RF circuit
TDMA circuit
1909
SRAM
1908
PLL circuit
ROM
1907
System control microcomputer
Liquid crystal module
Keyboard
1910
EEPROM
1905